DIGITAL TAPPED DELAY LINES FOR HWIL TESTING OF MATCHED FILTER RADAR RECEIVERS

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ABSTRACT

Matched filter processing for pulse compression of phase coded waveforms is a classic method for increasing radar range measurement resolution. A generic approach for simulating high resolution range extended radar scenes in a Hardware in the Loop (HWIL) test environment is to pass the phase coded radar transmit pulse through an RF tapped delay line comprised of individually amplitude- and phase-weighted output taps. In the generic approach, the taps are closely spaced relative to time intervals equivalent to the range resolution of the compressed radar pulse. For a range-extended high resolution clutter scene, the increased number of these taps can make an analog implementation of an RF tapped delay system impractical. Engineers at the U.S. Army Aviation and Missile Research, Development and Engineering Center (AMRDEC) have addressed this problem by transferring RF tapped delay line signal operations to the digital domain. New digital tapped delay line (DTDL) systems have been designed and demonstrated which are physically compact compared to analog RF TDLs, leverage low cost FPGA and data converter technology, and may be readily expanded using open slots in a VME card cage. In initial HWIL applications, the new DTDLs have been shown to produce better dynamic range in pulse compressed range profiles than their analog TDL predecessors.

This paper describes the signal requirements and system architecture for digital tapped delay lines. Implementation, performance, and HWIL simulation integration issues for AMRDEC's first generation DTDLs are addressed. The paper concludes with future requirements and plans for ongoing DTDL technology development at AMRDEC.

Keywords: Radar, Doppler, Simulation, Matched Filter Processing, Pulse Compression, Radar Scene Generation, Hardware-in-the-Loop

1.0 Introduction

In typical HWIL simulations of radar target and clutter environments for matched filter pulse compression seekers, an RF tapped delay system is used to generate the fine range profile of range-extended point scatterer models [1]. Analog versions of these systems have been successfully used at AMRDEC HWIL facilities since the mid 1980s. With appropriate scene

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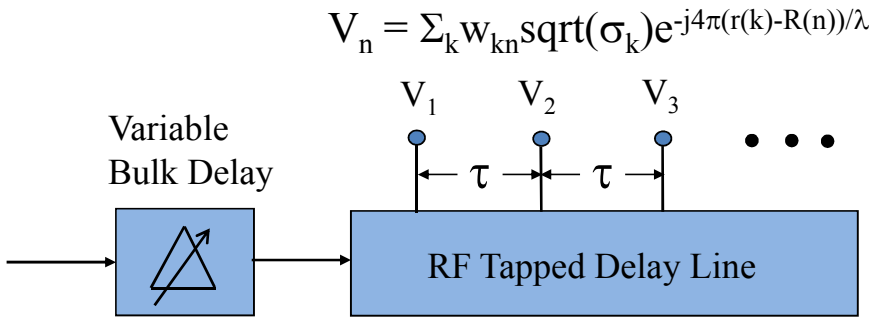
model computer resources and fast I/O interfaces for updates to tap weight amplitude and phase modulation signals, up to 16 tap configurations have been implemented from discrete RF components. These limited scale delay line systems have supported all previous tactical or air defense target models and ground clutter in up to eight seeker range gates. Newer seeker signal processing technology has created a need for larger TDL tap counts since many more range gates can now be computed and searched for targets.

2.0 Role of the Tapped Delay Line in HWIL RF Signal Generation System

In essence, the RF Tapped Delay Line system provides for a convolution of the range-extended series of scene model scatterer voltages with the frequency converted and delayed seeker transmit pulse. Scene model scatterers represent the decomposition (in space) of the complex reflectivity of target or clutter into discrete points with characteristic amplitude, phase in each polarization set. For a given LOS aspect on the radar scene, these scatterers are sorted by range into intervals bounded by delay line tap locations. A complex voltage is computed for each scatterer from its amplitude and path length phase, given range, and seeker transmit frequency. The resulting complex voltage is then weighted into tap modulation sums for each adjoining tap. A close match between real-world range profile measurement and HWIL simulation range profiles is achieved when the delay line tap interval is less than or equal to ½ the seeker pulse compression range resolution. Figure 1 illustrates the tap modulation weighting described.



τ = time delay equivalent to range interval <= ½ seeker minimum range resolution

Figure 1 - Tapped Delay Line Element within HWIL Signal Generation Chain Allows Convolution of Scene Model Scatterer Voltages With Seeker RF Pulses

3.0 DTDL System Design Requirements

Starting in 2002, the HWIL engineering staff at AMRDEC began a study of technology to support an all-digital replacement of existing RF tapped delay systems for tactical missile seeker testing. The basic design requirements established for the digital TDL system included both signal processing and computer interfacing characteristics. Key signal processing characteristics such as A/D and D/A conversion data word size, signal sample rate (related to both instantaneous RF bandwidth capability and time delay command resolution), output signal dynamic range, and scalability of the digital taps section beyond the initial 16 tap prototype configuration. Based on radar waveforms and pulse compression parameters of seekers slated for HWIL testing, a 10-bit A/D conversion front end sampling at 210MSPS was deemed adequate. This sample rate

supports both the pulse instantaneous bandwidth and tap spacing resolution based discrete intervals of sample period delays. Additional DTDL system design requirements are tabulated as follows:

Characteristic	Requirement	Addressing
Number of active taps:	4-128	Expected range extent of target model and/or clutter swath
Digital signal sample rate:	>=210 MSPS	Support for range gate spacing relation to DTDL clock period
Digital Hilbert Transform filter bandwidth	>= 80 MHz	Support for seeker pulse bandwidth
Maximum TDL delay	>=107uS (16Km range)	Support maximum MMW seeker operating range
Minimum (insertion) delay	<=300nS (45m added range)	Support minimum MMW seeker operating range
Minimum individual tap modulation dynamic range	55 dB	Predicted composite dynamic range for 3sigma Rayleigh variation and clutter shadowing
Tap weight command rate:	Ntaps x 2 polarizations x effective PRF	Time- or frequency-dependent scatterer phase generation pulse-to-pulse
Programmable tap spacing	5 and 10 meters spacing	Support HWIL delay resolution for coarse range gate simulations
High speed modeling interface to tap weight RAM buffers	RACE++ Interlink (based on modeling computer selection)	Pulse-to-pulse updates of tap weight values

Table 1: Summary of Design Requirements for Digital Tapped Delay Line System

The host computer system was an existing 9U VME bus real-time system built around Mercury Computer Systems RACE++ processor boards. As a result, the desired board format for the DTDL electronics was also 9U VME – with interface support for both VME bus and RACE++ interlink access. Since control of the DRFM electronics section of the DTDL system requires minimal data traffic, only VME bus slave access is implemented for that circuit board. To support expansion of the number of delay line taps, a modular sample data cable interface was defined for connection of a multiple digital taps board to the output signals from a single data conversion front end card. Figures 2a and 2b are photos of the prototype 9U VME board implementation of the DTDL circuitry.

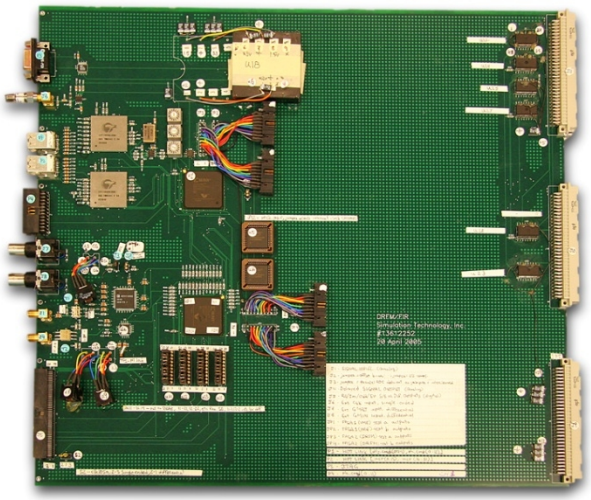


Figure 2a - DRFM/FIR Filter Board

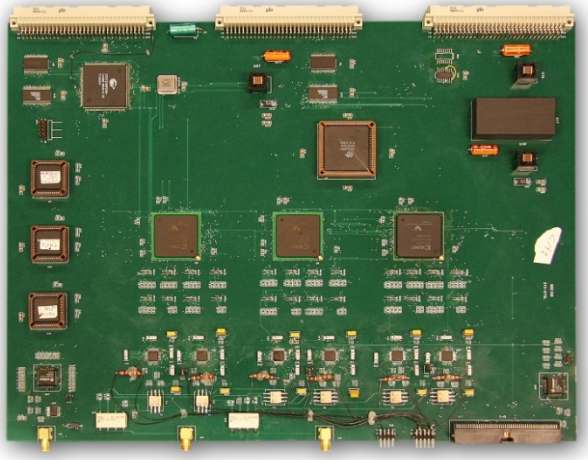


Figure 2b - Digital Taps Board

4.0 Implementation

The digital tapped delay system is divided into two major components. The front end subsystem is an analog signal sampling and bulk sample delay circuit on a printed circuit card termed the "DRFM/FIR" board. The back end subsystem provides a series of quadrature modulation tap cells for amplitude and phase modulation of tap output signals. These tap cells are located on one or more digital tap cards. The reconstructed analog outputs from D/A converters at digital tap cell outputs are further combined via analog summation to form the final tap system output signal for each polarization. Figure 3 show the major component sections of the DTDL system.

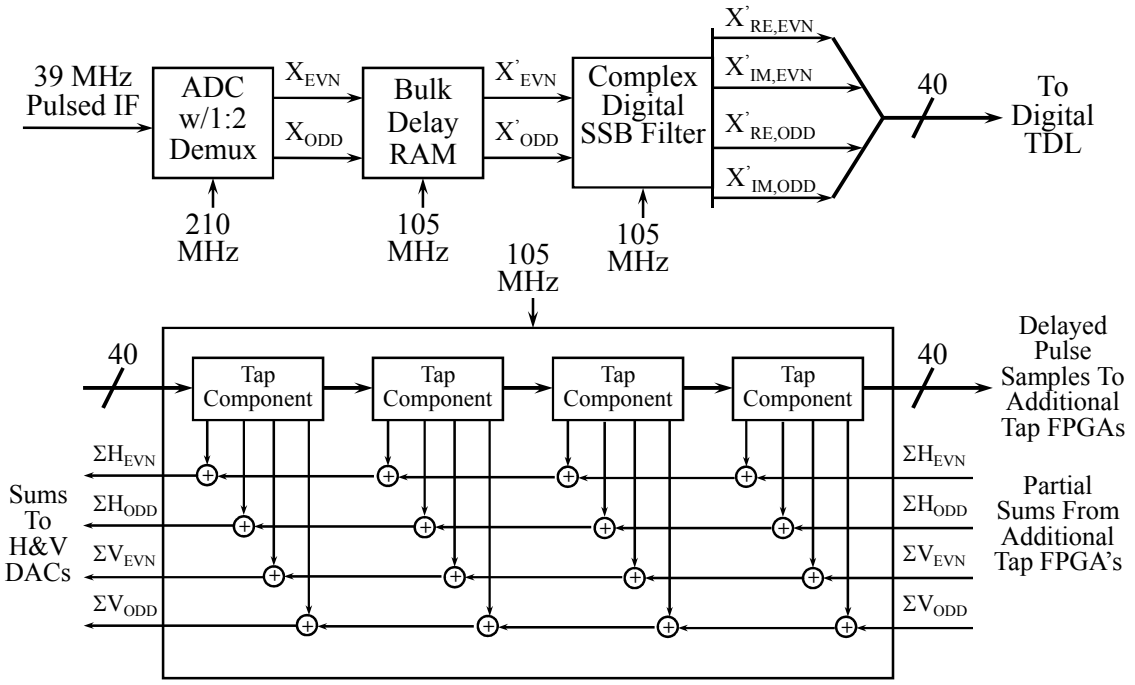


Figure 3 - DSP Sections of DTDL System Include DRFM/FIR and Digital Taps

4.1 DRFM/Hilbert FIR Filter Component

The DRFM/FIR board performs three basic functions: 1) sampling of the downconverted seeker transmit pulse at 210MSPS and demultiplexing the 10-bit even and odd time samples at 105MSPS, 2) delay of the demultiplexed signal samples in a programmable ring buffer (i.e. a Digital RF Memory, or DRFM) to create coarse time delay simulating range, and 3) application of a complex digital FIR filter to the real A/D samples of the radar pulse appearing at the output of the DRFM section. The complex digital FIR filter creates the harmonic conjugate (Hilbert Transform) of the real A/D signal in order to support amplitude and phase modulation at each tap cell via complex number multiplication. An important aspect of the Hilbert Transform implementation is the half rate form for the coefficient sets and filter network [3]. This allowed the filter computations to proceed at the reduced clock frequency of 105 MHz and preserved separate even and odd time sample streams (or sequences), greatly simplifying FPGA design for the devices used. The cost for half rate Hilbert Transform filter architecture was a doubling of filter insertion delay and consumption of twice the FPGA DSP resources. Figure 4 shows the network diagrams for the Hilbert Transform digital filters. Note the total of four networks in the half rate filter configuration. The classic equi-ripple filter synthesis algorithm of Parks and McClellan was used to produce the filter coefficients [2]. The typical (efficient) half-band implementation of Hilbert Transform filter for this application was avoided in order to preserve flexibility in designing transition band attenuation characteristics.

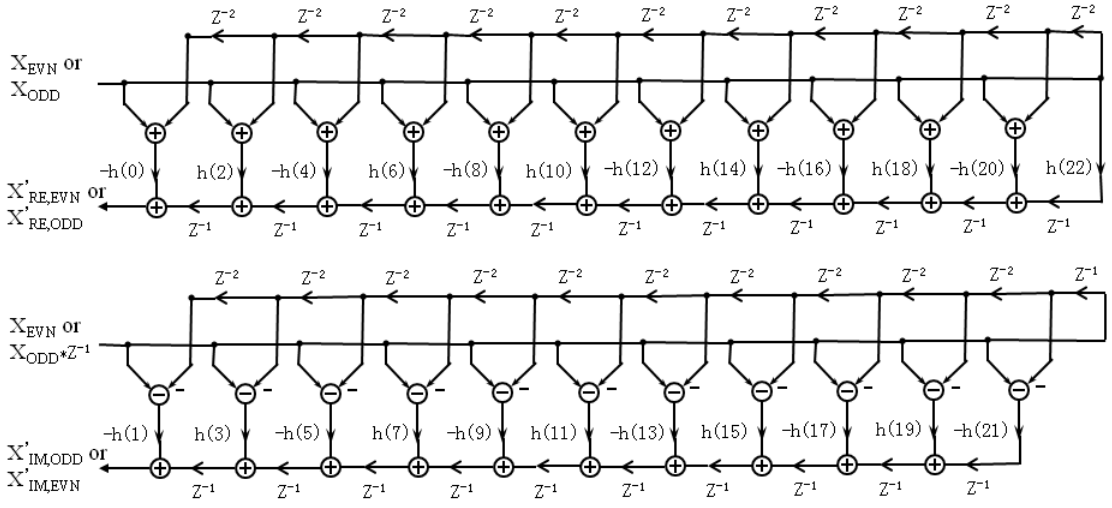


Figure 4 - Complex Bandpass Filter Networks Combine Hilbert Transform and SSB Modulator (Half Rate forms), and Reduced Multiplier Count for Symmetric Filter

4.2 Digital Taps Component

The Digital Taps board performs four basic functions: 1) distribution of the filtered complex number sample stream to multiple tap modulation cells at programmable intervals of tap-to-tap sample delay, 2) modulation of the pulse sample stream at each tap cell by complex number multiplication with a tap- and pulse-specific I/Q sample, 3) combination of digital signals from sets of four adjoining tap cells and reconstruction into analog form at 16-bit RF D/A converters, and 4) combination of reconstructed analog signals followed by programmable RF attenuation for coarse dynamic range control. Figure 5 provides some details of the digital tap cell architecture.

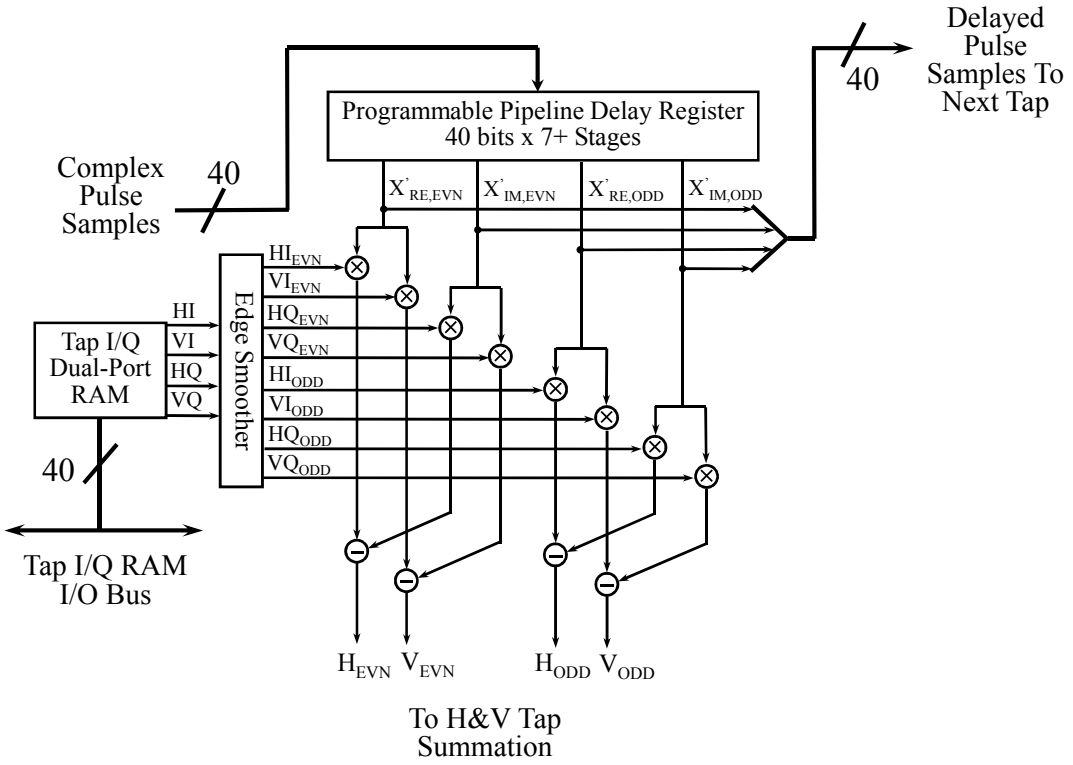


Figure 5 - Details of Digital Tap Cell

4.3 FPGA Implementation of DRFM/FIR and Digital Taps Components

All digital signal processing circuitry in the DTDL system is based on the Xilinx Virtex-4 FPGA family. The DRFM/FIR card implements all of its DSP in a single FPGA. The DRFM/FIR FPGA contains enough internal RAM to implement the required maximum range delay. The FPGA also contains enough logic in implement the four half-rate Hilbert Transform filter networks in addition to logic for DRFM delay control and test signal generation. The prototype Digital Tap Cell board incorporates three Virtex-4 FPGAs for tap cells and input/output digital signal routing. Tap cell complex number multiplications are implemented on the Virtex-4's hardware fixed point multiplier cores for maximum speed and minimum processing latency. Schematic capture logic design was used on the DRFM/FIR FPGA firmware project. HDL (VHDL) was used for logic synthesis of the digital tap cell FPGA firmware design based on its repetitive instances of data paths and math resources.

5.0 Testing and Demonstration

The DTDL System was successfully integrated in the Army AMRDEC/RTTC AMSTAR HWIL performance test facility during the 2005-2006 period and employed for RF seeker testing. Using initial VME bus I/O capability, both target models and ground clutter were simulated in a sensor guided closed loop flight simulation configuration. A qualitative assessment of DTDL operation shows that the system does not limit HWIL simulation performance. Seeker pulse compression of DTDL output signals are on a par with the analog TDL predecessor result. Figure 6 shows a pulse compressed range measurement of a single discrete scatterer modeled at one of the DTDL tap locations.

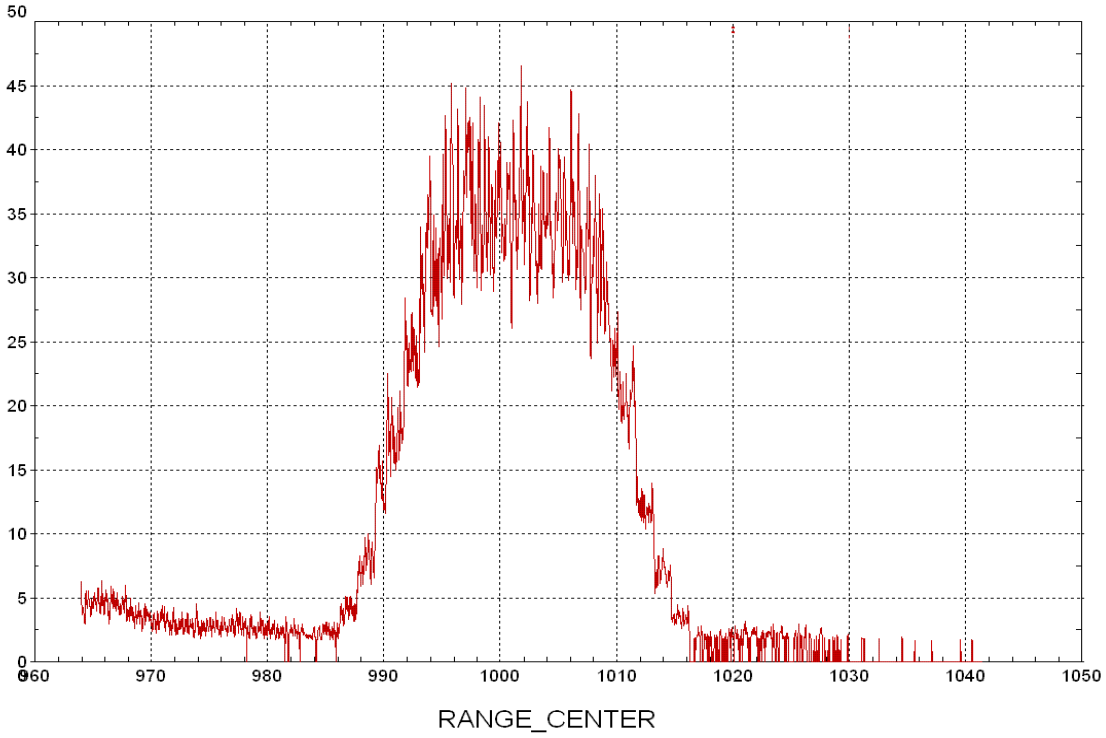


Figure 6 - Seeker Pulse Compression Response to DTDL is Similar to Analog TDL

6.0 Conclusion

An all-digital tapped delay system has been developed and demonstrated for multi-scatterer RF scene modeling in seeker HWIL simulations at the US Army AMRDEC. The new system successfully replaced much larger and more expensive analog tapped delay systems built up from discrete RF delays and amplitude/phase modulators. The new systems are expandable in terms of tap count and will employ high speed computer I/O interfaces such as Mercury RACE++ to support real-time updates of tap weights in larger tap count configurations. System calibration time is insignificant versus the older analog tapped delay systems. Follow-on designs for DTDLs are expected at AMRDEC with support for increased pulse bandwidth, reduced insertion delay (blind range characteristic) and faster tap command I/O protocols.

References

[1] McPherson, D.A, "Tapped Delay Line Implementations for Range Extended RF Target Models", Southeastcon '81. Conference Proceedings, 5-8 Apr 1981, Page(s): 892-894.
[2] Parks, T.W., and J. H. McClellan, "Chebyshev Approximation for Nonrecursive Digital Filters with Linear Phase", IEEE Transactions on Circuit Theory, Vol. Cr-19, No. 2, March 1972, pages 189-194.
[3] Rabiner, L.R. and R. E. Crochiere, Multirate Digital Signal Processing, Prentice Hall (1983).

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